AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 10, lines 6 through 23, with the following amended paragraph:

Fig. 5 is a more detailed block diagram of the DMA controller with the read data paths. The read data paths are similar to the write data paths except the data valid bits used in the write data paths may be omitted in the read data paths. Although shown in both Figs. 4 and 5, the DMA engine, BCU controller, CRB, BCU and memory are not duplicated for the read path. However, there are independent arbiters for the read and write data paths. The DMA engine 500 is informed by an arbiter 501 which channel is ready for transferring data from the memory 502 to a burst disassembly buffer 504. The arbiter may operate on a round robin basis or any other suitable basis, such as by assigning priorities to different channels, to service requests for data that may be pending from a client port, e.g., 506. Up to a fixed number of bytes, such as 512 bytes, are transferred in a burst to the burst disassembly buffer. For example, the SDRAM controller may handle groups of 4 256-bit words (up to 16), the BAB/BDB can then refine the granularity to individual 256-bit words, and the individual clients can then further refine the granularity to individual 32-bit words. The DMA controller loads the appropriate parameters for the transfer from the DMA context RAM block 508 and effects the data transfer using the ~~state information~~ RAM 512 about the buffer through the BCU controller 510, in a manner described below in connection with Figs. 6 and 7. After the data transfer is performed, the BCU controller is informed so that the state information about the buffer may be updated in the BCU context RAM block 512. The DMA controller also updates the active DCB.

Please replace the paragraph beginning on page 10, line 25 and ending of page 11, line 5, with the following amended paragraph:

There is a 5-bit counter 514 associated with each port's designated address range within the burst disassembly buffer 504. After up to sixteen 256-bit words (512 bytes) have been written into the address range for a channel in the burst disassembly buffer 504, that data may be read out through disassembly buffers 516 to the appropriate channel. An arbiter 520 controls which channel is reading from the burst disassembly

buffer 504 into its corresponding buffer, from which data is transferred to its corresponding channel. This arbiter may operate, for example, on a round robin basis, or other suitable scheme, such as by assigning different priorities to different channels. The disassembly buffers 516 receive and store each 256-bit word in a FIFO memory for a channel as indicated at 526. A counter 528 for each channel determines when the FIFO is full or empty. Data in the FIFO is transferred to the client port 506 in 4 consecutive 64-bit chunks. The transferred data may be subjected to appropriate padding and formatting ~~(indicated at 522) to~~ at the FIFO 524 at the client port 506. Similar to write operations, the DMA controller also may send information about the transfer to the port that is reading the data over the client control bus 530 to be used by the counter and control logic 532.